**Digital Signal Design Lab**

Lab CEL-442

Lab Journal: 6



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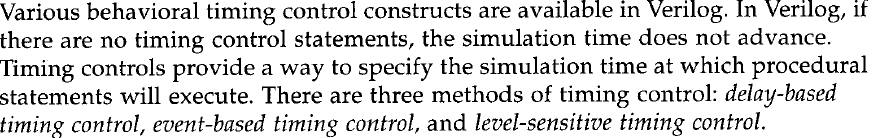
Class: BCE-06

Enrollment No: 01-132182-024

**Lab # 6**

**Title: Behavioral Modelling**

**Objective** This lab is aimed at **Timing Control**



**Introduction**

**Task 1:**

`timescale 1ns / 1ps

output out;

input i0, i1, i2, i3;

input s1, s0;

reg out;

always @(\*)

case (s1 & s0)//Switch based on concatenation of control signals

2'd0 : out = i0;

2'd1 : out = i1;

2'd2 : out = i2;

2'd3 : out = i3;

default: $display("Invalid control signals");

endcase

endmodule

**Testbench**

`timescale 1ns / 1ps

module mux\_4\_to\_1\_test;

// Inputs

reg i0;

reg i1;

reg i2;

reg i3;

reg s1;

reg s0;

// Outputs

wire out;

// Instantiate the Unit Under Test (UUT)

mux4\_to\_1 uut (

.out(out),

.i0(i0),

.i1(i1),

.i2(i2),

.i3(i3),

.s1(s1),

.s0(s0)

);

initial begin

// Initialize Inputs

i0 = 0;

i1 = 0;

i2 = 0;

i3 = 0;

s1 = 0;

s0 = 0;

// Wait 100 ns for global reset to finish

#100;

i0 = 1;

i1 = 1;

i2 = 1;

i3 = 1;

s1 = 1;

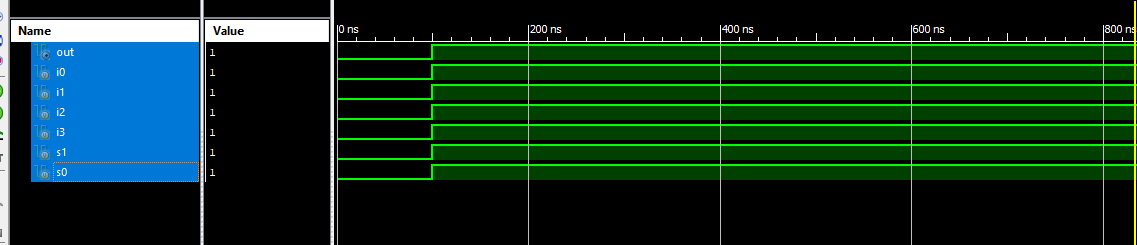
s0 = 1;

// Add stimulus here

end

endmodule

**OUTPUT:**



**Task 2**

`timescale 1ns / 1ps

module module\_abc(

);

`define TRUE 1'b1;

//'define TRUE 1'b1';

`define FALSE 1'b0;

//'define FALSE 1'b0;

reg [15:0] flag;

integer i; //integer to keep count

reg continue;

initial

begin

flag = 16'b 0010\_0000\_0000\_0000;

i = 0;

continue = `TRUE;

while ((i < 16) && continue ) //Multiple conditions using

begin

if (flag[i])

begin

$display("Encountered a TRUE bit at element number %d", i);

continue = `FALSE;

end

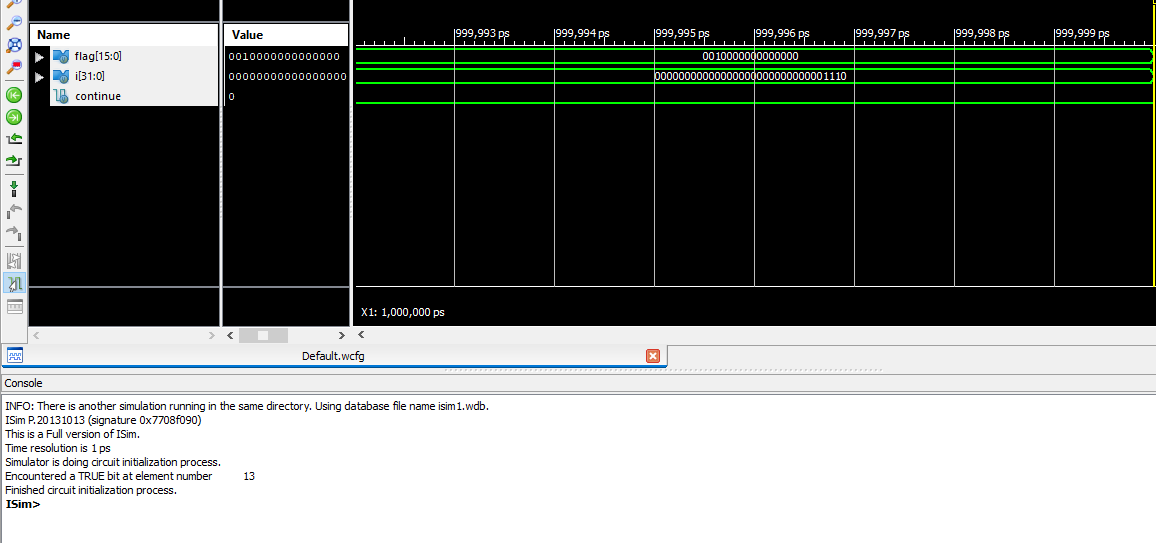
i = i + 1;

end

end

endmodule

**OUTPUT**



**Task 3**

`timescale 1ns / 1ps

module module\_xyz(

);

integer count;

initial

begin

count = 0;

while (count < 128)

$display("Count = %d", count);

count = count + 1;

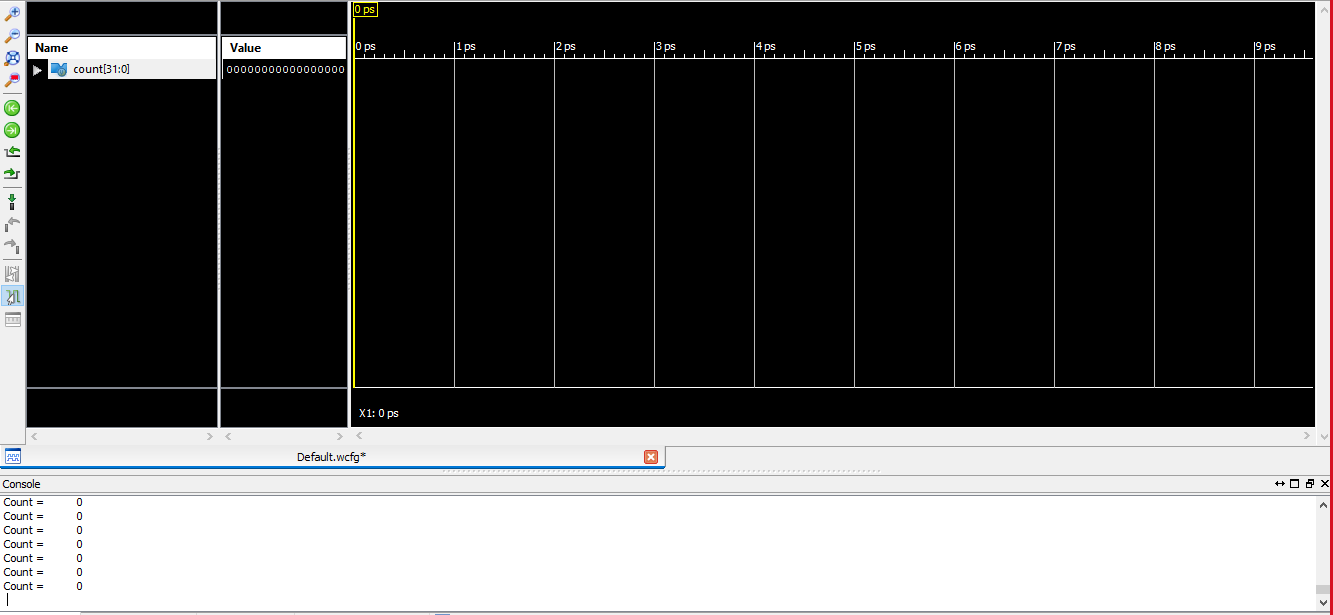
begin

end

end

endmodule

**OUTPUT :**



**Conclusion: -**

In this lab we learned about **Behavioral Modelling**